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UNITED STATES PATENT APPLICATION FOR

PACKAGED SEMICONDUCTOR DEVICE HAVING STACKED DIE

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PACKAGED SEMICONDUCTOR DEVICE HAVING STACKED DIE

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices.

- 5 More specifically, the present invention relates to an apparatus and method for forming a packaged semiconductor device having stacked die.

BACKGROUND ART

- Packaged semiconductor devices containing multiple semiconductor die provide high device density. In addition, packaged semiconductor devices containing multiple semiconductor die can provide increased functionality and performance.
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- Packaged semiconductor devices containing multiple semiconductor die typically include a first semiconductor die that is attached to a package substrate. Bonding pads are disposed around the periphery of the top surface of the first semiconductor die. Wire bonds electrically connect to the bonding pads on the first semiconductor die and electrically connect to corresponding bonding pads located on the package substrate. The spacer is then attached to the center of the top surface of the first semiconductor die.
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The second semiconductor die is attached to the spacer. Bonding pads disposed on the top surface of the second semiconductor die are then electrically connected to bonding pads on the package substrate using wire

bonds. Encapsulant is then applied so as to cover the semiconductor die and all of the wire bonds.

The manufacturing process for forming packaged semiconductor devices containing multiple semiconductor die is expensive. More particularly, spacers add cost to the manufacturing process. In addition, the spacer must be precisely placed so as to prevent damage to wire bonds.

Also, it is difficult to apply encapsulant such that the encapsulant will completely fill the areas surrounding the spacer. Often, air is trapped under the second semiconductor die in the areas surrounding the spacer. This causes voids within the encapsulant in the areas surrounding the spacer. This leads to a packaged semiconductor device having reduced structural integrity. Also, the voids can trap moisture, leading to reliability problems.

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What is needed is a packaged semiconductor device and a method for forming a packaged semiconductor device having improved structural integrity and reliability. Also, a method and apparatus is needed that meets the above need while reducing manufacturing cost. The present invention meets the above needs.

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DISCLOSURE OF THE INVENTION

The present invention provides a method for forming a packaged semiconductor device and a packaged semiconductor device in which encapsulant is used for separating stacked semiconductor die. The method and apparatus of the present invention reduces manufacturing cost while
5 improving structural integrity and reliability.

A method for forming a packaged semiconductor device having stacked die and a packaged semiconductor device having stacked die are
10 disclosed. A first semiconductor die is coupled to a ball grid array substrate. Wire bonds are then coupled to the first semiconductor die and to the ball grid array package substrate so as to electrically couple the first semiconductor die to the ball grid array package substrate.

15 Encapsulant is disposed over the first semiconductor die and over the wire bonds. The encapsulant is then at least partially cured. The encapsulant completely fills the area surrounding the first semiconductor die. Accordingly, no air pockets are formed that can cause integrity problems or reliability problems as can occur in prior art processes that use spacers.

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A second semiconductor die is coupled to the encapsulant. In one embodiment, the second semiconductor die at least partially overlies the first semiconductor die. The second semiconductor die is then electrically coupled to the ball grid array substrate.

Encapsulant is then applied and cured to form a second layer of encapsulant that covers the second semiconductor die. The second layer of encapsulant completely fills the area surrounding the second semiconductor die. Accordingly, no air pockets are formed that can cause integrity problems or reliability problems as can occur in prior art processes that use spacers.

Because a spacer is not required, the method and apparatus of the present invention results in cost savings. Moreover, because the method and apparatus of the present invention does not result in the formation of voids, reliability and structural integrity problems are avoided as compared to prior art processes that use spacers.

These and other advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments, which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

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FIGURE 1 is a flow chart that illustrates a method for forming a packaged semiconductor device in which die are stacked and in which encapsulant separates adjoining die in accordance with one embodiment of the present invention.

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FIGURE 2 shows a cross-sectional view of a semiconductor die coupled to a ball grid array package substrate in accordance with one embodiment of the present invention.

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FIGURE 3 is a top view of the structure of Figure 2 after wire bonds have been coupled to the semiconductor die and to the ball grid array package substrate in accordance with one embodiment of the present invention.

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FIGURE 4 is a cross-sectional view of the structure of Figure 3 along cross section A-A in accordance with one embodiment of the present invention.

FIGURE 5 is a top view of the structure of Figure 3 after encapsulant has been applied and cured so as to form a first layer of encapsulant in accordance with one embodiment of the present invention.

5 FIGURE 6 is a cross-sectional view of the structure of Figure 5 along cross section B-B in accordance with one embodiment of the present invention.

FIGURE 7 is a cross-sectional view of the structure of Figure 6 after a
10 second semiconductor die has been coupled to the first layer of encapsulant in accordance with one embodiment of the present invention.

FIGURE 8 is a cross-sectional view of the structure of Figure 7 after the second semiconductor die has been electrically coupled to the ball grid
15 array package substrate using wire bonds in accordance with one embodiment of the present invention.

FIGURE 9 is a top view of the structure of Figure 8 in accordance with one embodiment of the present invention.

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FIGURE 10 is a cross-sectional view of the structure of Figure 8 after encapsulant has been applied and cured so as to form a packaged semiconductor device in accordance with one embodiment of the present invention.

FIGURE 11 is a top view of the structure of Figure 10 in accordance with one embodiment of the present invention.

- 5 The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

Figure 1 illustrates a method 100 for forming a packaged semiconductor device. As shown by step 101 a first semiconductor die is coupled to a package substrate. In the present embodiment, the first semiconductor die is coupled to the package substrate using adhesive. The package substrate can be a ball grid array package substrate. Alternatively, other types of package substrates could be used.

In one embodiment, adhesive is applied and the first die is placed over the package substrate in a first process step. The adhesive is then cured in a subsequent heating process step. The adhesive can be either a liquid or a solid adhesive (e.g., an adhesive tape). In one embodiment, a semiconductor die-attach adhesive is used that is formulated for attachment of semiconductor die. In one embodiment, the adhesive is a liquid polymer epoxy that is thermally conductive such as, for example, silver-filled epoxy.

Figure 2 shows an embodiment in which a semiconductor die 12 is coupled to a ball grid array package substrate 10. In this embodiment, adhesive layer 14 is disposed between semiconductor die 12 and ball grid array package substrate 10. Adhesive layer 14 attaches semiconductor die 12 to ball grid array package substrate 10.

As shown by step 102 of Figure 1, wire bonds are coupled to the first semiconductor die and to the package substrate. This first set of wire bonds electrically couples the first semiconductor die to the package substrate. In the present embodiment an automated wire bonding apparatus is used for coupling wire bonds to the first semiconductor die and to the package substrate.

Referring now to Figure 3, semiconductor die 12 is shown to include bonding pads 17. In the present embodiment, bonding pads 17 are disposed on the top surface of semiconductor die 12 around the periphery of

semiconductor die 12. Internal region 40 is indicated which is that portion of the top surface of semiconductor die 12 that lies inside of bonding pads 17.

Continuing with Figure 3, ball grid array package substrate 10 includes
5 bonding pads 18 that are disposed on a portion of ball grid array package substrate 10 that is raised relative to the center portion of ball grid array package substrate 10 to which semiconductor die 12 is attached. Ball grid array package substrate 10 also includes bonding pads 19 that are disposed on a portion of ball grid array package substrate 10 that is raised relative to
10 bonding pads 18. It is appreciated that the number and placement of bonding pads 17-19 is illustrative and that the present invention is well adapted for the use of more or fewer bonding pads 17-19 and different placement of bonding pads 17-19.

15 Referring now to Figures 3-4, ball grid array package substrate 10 is shown to include an array of solder balls 11 that are disposed on the top surface of ball grid array package substrate 10. Solder balls 11 electrically couple to ones of bonding pads 18-19. It is appreciated that the number and placement of solder balls in the present embodiment is illustrative and that the
20 present invention is well adapted for the use of more or fewer solder balls 11 and different placement of solder balls 11. In one alternate embodiment, solder balls 11 are disposed on the bottom surface 19 of ball grid array package substrate 10.

Continuing with Figures 3-4, wire bonds 16 couple bonding pads 17 of semiconductor die 12 to bonding pads 18 of ball grid array package substrate 10. Thereby, wire bonds 16 electrically couple the circuitry of semiconductor die 12 to solder balls 11.

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Referring to step 103 of Figure 1, encapsulant is applied. In the present embodiment, encapsulant is applied such that the encapsulant is disposed over both the first semiconductor die and the wire bonds. In the embodiment shown in Figures 5-6, encapsulant is applied within the central portion of ball grid array package substrate 10 such that all of bonding pads 17-18 and wire bonds 16 are completely covered.

As shown by step 104 of Figure 1, the encapsulant is cured. In one embodiment the encapsulant is fully cured. In another embodiment, the encapsulant is only partially cured.

The curing process varies depending on the type of encapsulant used. In one embodiment, an epoxy-based polymer encapsulant is used that is fully cured by heating the encapsulant for a time specified by the encapsulant manufacturer. In one embodiment, an epoxy-based polymer encapsulant is used that is partially cured by heating the encapsulant for seventy-five percent of the amount of time specified by the encapsulant manufacturer.

Referring now to Figures 5-6, once the curing process is completed an encapsulant layer 20 is formed that completely covers semiconductor die 12, and completely covers each of wire bonds 16. Encapsulant layer 20 protects and insulates semiconductor die 12 and wire bonds 16. Accordingly,
5 semiconductor die 12 and wire bonds 16 are protected and are not damaged in subsequent process steps. Also, because there is no spacer and no overlying semiconductor die to trap air, voids do not form within encapsulant layer 20 as occurs in prior art fabrication processes that use spacers.

10 Referring now to step 105 of Figure 1, the second semiconductor die is coupled to the first encapsulant layer. In the present embodiment, the second semiconductor die is coupled to the first encapsulant layer using adhesive. In the embodiment shown in Figure 7, semiconductor die 22 is shown to be attached to layer of encapsulant 20 by adhesive layer 24.

15 In one embodiment, the uncured adhesive is applied and the second semiconductor die 22 is placed over the encapsulant layer 20 in a first process step. The adhesive is then cured in a subsequent heating process step.

20 Adhesive layer 24 can be formed using either a liquid or a solid adhesive (e.g., an adhesive tape). In one embodiment, the same adhesive is used that is used in step 101 of Figure 1. However, a different adhesive could also be used. In the present embodiment, a thermally conductive liquid

polymer die-attach adhesive is used such as, for example, silver-filled epoxy adhesive.

In the present embodiment, semiconductor die 22 is shown to be
5 disposed over semiconductor die 12 such that semiconductor die 22
completely overlies semiconductor die 12. However, alternatively,
semiconductor die 22 could be offset such that it only partially overlies
semiconductor die 12. In yet another embodiment, semiconductor die 22
could be offset such that it does not overlie semiconductor die 12 at all.

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Because layer of encapsulant 20 fully supports semiconductor die 22,
and separates semiconductor die 22 from semiconductor die 12, there is no
need for a separate supporting structure (e.g., a spacer) as is used in prior art
fabrication processes. Accordingly, in the method and apparatus of the
15 present invention, no supporting structure (e.g., a spacer) extends between
semiconductor die 12 and semiconductor die 22. Referring to Figure 7, only
encapsulant (portions of encapsulant layer 20) and adhesive (portions of
adhesive layer 14) are disposed above the top surface of semiconductor die
12, within internal region 40 (Figure 3), and below semiconductor die 22.

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As shown by step 106 of Figure 1, wire bonds are coupled to the
second semiconductor die and coupled to the package substrate. This
second set of wire bonds electrically couples the second semiconductor die to
the package substrate.

In the embodiment shown in Figures 8-9, semiconductor die 22 is shown to include bonding pads 27 that couple to the internal circuitry of semiconductor die 22. In the present embodiment, bonding pads 27 are
5 disposed on the top surface of semiconductor die 12 around the periphery of semiconductor die 22.

Continuing with Figures 8-9, wire bonds 26 are coupled on one end to bonding pads 27 and coupled on the opposite end to ones of bonding pads
10 19. Wire bonds 26 electrically couple bonding pads 27 of semiconductor die 22 to bonding pads 19 of ball grid array package substrate 10. Thereby, wire bonds 26 electrically couple the circuitry of semiconductor die 22 to solder balls 11.

15 Referring now to step 107 of Figure 1, encapsulant is applied. In the present embodiment, encapsulant is applied such that the encapsulant is disposed over both semiconductor die 22 and wire bonds 26. In the embodiment shown in Figures 8-9, encapsulant is applied within the central portion of ball grid array package substrate 10 such that all of bonding pads
20 27, bonding pads 19 and wire bonds 26 are completely covered.

As shown by step 108 of Figure 1, the encapsulant is cured. In the present embodiment the encapsulant is fully cured. The curing process varies depending on the type of encapsulant used. In one embodiment, an

epoxy-based polymer encapsulant is used that is fully cured by heating the encapsulant for a time specified by the encapsulant manufacturer.

When the encapsulant applied in step 103 is only partially cured in step 5 104, better adhesion can result between the top surface of the encapsulant applied in step 103 and the bottom surface of the encapsulant applied in step 107. However, depending on the type of encapsulant used for performing step 103 and the type of encapsulant used for performing step 107, partial curing may or may not be required. Moreover, depending on the type of 10 encapsulant used for performing step 103 and the type of encapsulant used for performing step 107, the amount of partial curing will vary.

Referring now to Figures 10-11, once the curing process is completed, an encapsulant layer 30 is formed that completely covers semiconductor die 15 22, and completely covers each of wire bonds 26. Because there is no spacer and no overlying semiconductor die to trap air, voids do not form within encapsulant layer 20 as occurs in prior art fabrication processes that use spacers.

20 Because voids do not form within encapsulant layers 20 and 30, the method and apparatus of the present invention avoids the reliability problems and integrity problems that occur in prior art fabrication processes that use spacers. Also, by forming a first encapsulant layer 20 that covers die 12 and wire bonds 16, prior to performing steps 105-108, die 12 and wire bonds 16

are protected during process steps 105-108. This results in higher manufacturing yield and lower defect rates.

In the method and apparatus of the present invention no spacer is
5 required for separating the first semiconductor die from the second semiconductor die. This results in cost savings as there is no need to procure or precisely locate a spacer as is required in prior art assembly methods. In addition, the method and apparatus of the present invention does not result in voids that can trap air as occurs in prior art assembly methods. Accordingly,
10 reliability and structural integrity of the resulting packaged semiconductor device is improved.

In the present embodiment, adhesive layers 14, 24 and encapsulant layers 20, 30 are disclosed to be epoxy. However, the nature of the epoxy
15 that is an adhesive is fundamentally different in its characteristics from the epoxy that is an encapsulant. More particularly, the primary function of an adhesive is to adhere to and attach adjoining structures. In contrast, the primary function of encapsulant is to enclose, insulate and protect.

20 Method 100 is illustrated in Figures 1-11 as being applied for forming a stacked-die structure that includes only two die. However, additional stacked-die could be added by repeating steps 105-108 for each subsequent die. Thereby, packaged semiconductor devices having three, four, or even more stacked die could be formed.

The preferred embodiment of the present invention is thus described.
While the present invention has been described in particular embodiments, it
should be appreciated that the present invention should not be construed as
5 limited by such embodiments, but rather construed according to the following
claims.